

Page



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/046,754	01/17/2002	Masaki Okuda	107337-00006	2642

7590 02/25/2004

ARENT FOX KINTNER PLOTKIN & KAHN, PLLC
Suite 600
1050 Connecticut Avenue, N.W.
Washington, DC 20036-5339

EXAMINER

BAKER, PAUL A

ART UNIT	PAPER NUMBER
----------	--------------

2188

DATE MAILED: 02/25/2004

4

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/046,754

Applicant(s)

OKUDA, MASAKI

Examiner

Paul A Baker

Art Unit

2188

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 17 January 2002.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-9 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1,3,5,6 and 9 is/are rejected.
- 7) ☒ Claim(s) 2,4,7,8 is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☒ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date 3.
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____.

DETAILED ACTION

Specification

The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

Double Patenting

The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and, *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

Claims 1,3,5,6,9 are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claim 1 of U.S. Patent No. 6,421,292 ('292) in view of claim 1 of US Patent 6,529,435 ('435).

In regards to claim 1, a data inputting circuit for receiving data inputted from an external circuit is inherent to all memories for their proper operation, data must be inputted into the memory in order for the memory to store the data. '292 claim 1 contains a parity generating circuit for generating parity data from the data input from said data inputting circuit on lines 2 and 3;

a memory for storing the data input from said data inputting circuit and the parity data generated by said parity generating circuit is shown in '292 claim 1 lines 4-9;

a refreshing circuit for refreshing said memory is shown in '435 claim 1 lines 9-12;

a reading circuit for reading the data from said memory is shown in '435 claim 1 lines 5-8;

a restoring circuit for restoring data to be refreshed by said refreshing circuit from other data read normally and corresponding parity data, while said reading circuit is reading data is shown in '435 claim 1 lines 16-21;

a data outputting circuit for outputting the data read by said reading circuit and the data restored by said restoring circuit is shown in '435 claim 1 lines 5-8;

and a parity outputting circuit for directly reading and outputting the parity data stored in said memory is inherent for the data restoration function to occur, the parity data must be read to restore the data.

'292 and '435 are commonly assigned to applicant, it is obvious to combine both said patents because both use parity to generate data when a read is received during a refresh operation.

In regards to claim 3, a data inputting circuit for receiving data inputted from an external circuit is inherent to all memories for their proper operation, data must be inputted into the memory in order for the memory to store the data. '292 claim 1

Art Unit: 2188

contains a parity generating circuit for generating parity data from the data input from said data inputting circuit on lines 2 and 3;

a memory for storing the data input from said data inputting circuit and the parity data generated by said parity generating circuit is shown in '292 claim 1 lines 4-9;

a refreshing circuit for refreshing said memory is shown in '435 claim 1 lines 9-12;

a reading circuit for reading the data from said memory is shown in '435 claim 1 lines 5-8;

a restoring circuit for restoring data to be refreshed by said refreshing circuit from other data read normally and corresponding parity data, while said reading circuit is reading data is shown in '435 claim 1 lines 16-21;

a data outputting circuit for outputting the data read by said reading circuit and the data restored by said restoring circuit is shown in '435 claim 1 lines 5-8;

a writing circuit for directly writing desired data supplied from an external circuit in an area of said memory where said parity data is stored is inherent for storing parity data into memory from the said parity generating circuitry.

'292 and '435 are commonly assigned to applicant, it is obvious to combine both said patents because both use parity to generate data when a read is received during a refresh operation.

In regards to claim 5, a parity outputting circuit for directly reading and outputting the parity data stored in said memory is inherent for the data restoration function to occur, the parity data must be read to restore the data.

In regards to claim 6, a data inputting circuit for receiving data inputted from an external circuit is inherent to all memories for their proper operation, data must be inputted into the memory in order for the memory to store the data. '292 claim 1 contains a parity generating circuit for generating parity data from the data input from said data inputting circuit on lines 2 and 3;

a memory for storing the data input from said data inputting circuit and the parity data generated by said parity generating circuit is shown in '292 claim 1 lines 4-9;

a refreshing circuit for refreshing said memory is shown in '435 claim 1 lines 9-12;

a reading circuit for reading the data from said memory is shown in '435 claim 1 lines 5-8;

a restoring circuit for restoring data to be refreshed by said refreshing circuit from other data read normally and corresponding parity data, while said reading circuit is reading data is shown in '435 claim 1 lines 16-21;

a data outputting circuit for outputting the data read by said reading circuit and the data restored by said restoring circuit is shown in '435 claim 1 lines 5-8;

a control circuit for controlling said refreshing circuit to refresh circuit to refresh a given area according to a request from an external circuit is inherent to all DRAM

memories, in order to reduce the number of wait states in DRAM memories, DRAM refresh operations are triggered by signals external to the memory.

In regards to claim 9, a writing circuit for directly writing desired data supplied from an external circuit in an area of said memory where said parity data is stored is inherent for storing parity data into memory from the said parity generating circuitry.

Allowable Subject Matter

Claims 2, 4, 7, 8 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Paul A Baker whose telephone number is (703)305-3304. The examiner can normally be reached on M-F 10am-6:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mano Padmanabhan can be reached on (703)306-2903. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

PB

Mano Padmanabhan
2/23/04
MANO PADMANABHAN
SUPERVISORY PATENT EXAMINER
TC2100